APPLICATION

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APPLICANT NAME: Biggs et al

TITLE: METHOD OF FORMING A BOND PAD ON AN I/C CHIP AND RESULTING STRUCTURE

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METHOD OF FORMING A BOND PAD ON AN I/C CHIP AND RESULTING STRUCTURE

FIELD OF THE INVENTION

The invention generally relates to manufacturing integrated circuit (I/C) chips and, more particularly, to a technique for forming wire bonded I/C chips, and the resulting structure.

BACKGROUND OF THE INVENTION

Wire bonding is well-known in the art and used widely to interconnect chips with chip carriers. Traditionally, a gold wire is bonded to an aluminum pad. There are several limitations of this method. The intermetallics formed between gold and aluminum may reduce the reliability of the bond. Additionally, the robustness of the bonding process is compromised by bonding dissimilar metals. In advanced CMOS technology, copper metallization and low-k dielectrics, e.g. FSG (fluorinated silica glass), SiLK (a polyarelene ether by Dow Chemical), are used and, for even more advanced applications, porous, very weak materials are employed. This stage is sometimes referred to as the Back End of the Line (BEOL). The BEOL circuit structure is low modulus and sensitive to damage by pressure. The top aluminum surface, normally covered by a layer of oxide, must be removed in order to form a good contact between the test probe and the pad metal. This probe movement is called "scrubbing" or "plowing". Therefore, the chip is subjected to potential mechanical damage. It is highly desirable to establish an I/O pad that does not require scrubbing to provide low contact resistance with test probes. Currently, because of the need to "plow" into top aluminum, the pad size has to be quite large. This limits the chip design for higher I/O counts or results in an increased chip

size. The pad size is often double the size needed for bonding, since the probing area can become so damaged that it cannot be used for bonding.

SUMMARY OF THE INVENTION

A method of forming a wire bond structure in an integrated circuit (I/C) chip comprising the steps of: providing an I/C chip having a conductive pad for attaching to a wire bond with at least one layer of dielectric material overlying the pad for the wire bond; then forming an opening through said at least one layer of dielectric material to expose a portion of said pad for said wire bond. Thereafter, forming at least a first conductive layer on said exposed surface of said pad for said wire bond and on the surface and in the said opening in said layer of dielectric material, and then forming a seed layer on said first conductive layer. Then applying a photoresist material over said seed layer, exposing and developing said photoresist layer to reveal the surface of said seed layer surrounding said opening in said dielectric material, removing the exposed seed layer, and removing the photoresist material in said opening to reveal the seed layer thereunder. Then plating at least one layer of conductive material on said seed layer in said opening, and removing the remaining portion of said first conductive layer of conductive material on said dielectric layer around said opening. The invention also includes the resulting structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1-8 show schematically the steps in forming a wire bond connection on an I/C chip according to this invention;

Figure 9 is a photomicrograph of the plated Ni/Au wire bond pad; and

Figure 10 is a photomicrograph of the side wall of the Ni/Au wire bond pad.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

Referring now to the drawings, and for the present to Figure 1, a portion of an I/C chip 10 at the stage of production where a wire bond pad is to be formed is shown. Only the topmost layers and only one half of the pad area of the chip are shown. Also, the method described herein is performed at the wafer level. This stage is sometimes referred to as the Back End Of the Line (BEOL). The chip 10 includes an SiO_2 or other dielectric layer 12, typically about 0.5um thick, with an Si_3N_4 layer 14, typically about 0.5um thick, thereon. A layer of aluminum 16, typically 1 to 2um thick, is deposited on the layer 14, which Al layer 16 has an extension 18 extending through opening 20 in layers of SiO_2 12, and $Si_3N_4$14. Another layer of SiO_2 or other dielectric material 22, typically about 0.5um thick, is deposited on an Si_3N_4 layer and on the aluminum layer 18, and another layer 24 of Si_3N_4, typically about 0.5um thick, is deposited on SiO_2 layer 22. A layer of dielectric material, preferably a polyimide and more preferably a photosensitive polyimide 30, typically about 6um thick, is deposited over the layer 24 of Si_3N_4, and an opening 32 is formed through the polyimide 30, the Si_3N_4 layer 24 and the SiO_2 layer 22. If the polyimide is photosensitive, preferably the opening 32 is formed by conventional expose and develop techniques. If the polyimide 30 is not photosensitive, the opening 32 is preferably formed by a method using laser and mask. As indicated earlier, this represents the stage of formation of a portion of the I/C chip 10 when it is ready to have the wire bond pad formed according to this invention. Since the processing

of the chip to this point can be conventional, such processing need not be described in any detail.

Figures 2-8 depict the various steps in forming the wire bond pads according to this invention. Referring now to Figure 2, layers of TaN /Ta 36 and Cu 38 are sputter deposited by techniques, familiar to those versed in the art, on the layer of polyimide 30, and in the opening 32 included on the exposed surface of the Al layer 16 and the sidewalls of the opening 32. The sputtering process is conventional, with the TaN being deposited first, about 100A to 800A, and then the Ta, also about 100A to 800A, to form the TaN/Ta layer 36, then the Cu layer 38 (about 1500A to 5000A). The Cu will act as a seed layer for electro-deposition of metal, as will be described presently. It is also believed that, during the sputter deposition process of the TaN/Ta, the top surface of the polyimide 30 is carbonized to form a thin layer of carbonaceous material 40. Since this carbonaceous material is conductive (as opposed to the polyimide itself), when current is applied, the carbonaceous material will add to the conductivity of the layers 36 and 38, as will be explained presently.

Referring now to Figure 3, a photoresist 44 is applied over the copper layer 38, typically about 0.5 to 3.0um thick, and photopatterened and developed in a conventional manner to reveal all of the copper layer 38, except that which is in the opening 32. Although either positive or negative photoresist can be used, positive is preferred since it works well with copper, which is the seed layer.

Referring now to Figure 4, the exposed copper seed layer is removed, preferably by electroetching. This is a conventional process and techniques for this are shown in U.S. patents, e.g. by Datta et al in U.S. 5,486,282, and by Dinan et al in U.S. 5,536,388.

The photoresist in the opening 32 is removed by a conventional process, such as in a strong base to produce the structure shown in Figure 5, which has the copper seed layer 38 remaining only in the opening 32.

Referring now to Figure 6, layers of Ni 48, then gold 50, are electroplated onto the revealed copper seed layer 38 in opening 32. The electroplating process is conventional, using the TaN/Ta layer 36, the carbonaceous layer 40 and the copper layer 38, where it exists as electrical conductors. Thus, the carbonizing of the surface of the polyimide 30 has a positive, beneficial effect for electroplating. Electroplating or electrochemical deposition, is widely used in the industry to deposit metals on wafers or substrates. A cathodic current is applied to a wafer surface in either a nickel or gold plating tank. Based on plating time and applied currents, the amount of metal plated is controlled. The Ni is plated to a thickness of about 0.2 to 2 microns, and the Au is plated to a thickness of about 0.2 to 1 micron. The plating takes place only on the Cu layer 38, and not on the TaN/Ta layer 36. Also, the plating of the Au preferably takes place immediately after the Ni plating to avoid any possible oxidation of the Ni. The plating ceases when the configuration has reached that shown in Figure 6, and only minimally overlies the surface of the polyimide 30 surrounding the opening 32. Thus, as can be seen in Figure 6, an augmented bond pad of TaN/Ta/Cu/Ni/Au is provided in the opening 32 which includes the side walls as well as the bottom of the opening 32. Therefore,

assuming that the size of the original Al bond pad 16 exposed in the opening 32 is 92 microns x 48 microns, by using the side walls of the opening, the conductive area of the original bond pad is augmented by more than 30%, e.g. about 38%.

Referring now to Figure 7, the remaining TaN/Ta layer and remaining carbonaceous layer 40 are removed by plasma etching in a CF_4 based plasma using a standard etch tool to remove the TaN/Ta layer 38 and an oxygen plasma to remove the carbonaceous layer 40. The chip is now ready to receive a gold ball bond 52 and wire 54 as shown in Figure 8. The gold bond is comprised of the gold ball 52 which is formed by heating the gold wire 54 as is commonly practiced in the art. The bonding is preferably done by ultrasonic techniques, pressing the wire 54 and the ball 52 into the bond pad. This results in a strong, electrically efficient bond of the wire 54 to the Au of the Ni/Au layer 48 as shown in Figures 9 and 10. For illustration purpose, as noticed in Figure 10, only one sidewall is covered with gold metal. Ideally, all sidewalls are covered to maximize the bonding surface.